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10/734,162	12/15/2003	Ji Yong Park	P4274US00	2087

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H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

EXAMINER	
KIM, JAY C	

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Office Action Summary	Application No.	Applicant(s)	
	10/734,162	PARK ET AL.	
	Examiner	Art Unit	
	JAY C. KIM	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7 and 9-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7 and 9-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to RCE filed March 2, 2011.

Claim Objections

1. Claim 7 is objected to because of the following informalities: "the" should be inserted before "outer sides" on line 6. Appropriate correction is required.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "lightly doped drain (LDD) or offset regions" recited in claim 6 and "offset regions" recited in claim 7 whose outer sides "directly contacting the source and drain regions" must be shown or the feature canceled from the claim, because Fig. 6 of current Application includes regions between the LDD or offset regions II and the source/drain region 13a. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings

for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1 and 3-5 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Regarding claim 1, Applicants did not originally disclose that Fig. 6 of current Application is drawn to a scale - in fact Fig. 6 is a schematic illustration of primary crystal grain boundaries - and therefore did not originally and *specifically* disclose that "a width of each one of the offset regions is smaller than a distance between the primary crystal grain boundaries formed in the channel region”. (1) The evidence that Fig. 6 of current Application is a schematic illustration is found that all the primary crystal grain boundaries are straight lines, which are not physically possible when viewed at an atomistic scale. (2) Also, Applicants did

not originally disclose that all the primary crystal grain boundaries are equidistant from each other, which may not be enabling, and therefore one of ordinary skill in the art cannot determine a distance between the primary crystal grain boundaries formed in the channel region I from Fig. 6. (3) Further, scales of a cross sectional view in Fig. 5 of current Application is different from a plan view in Fig. 6 of current Application for relative lengths or widths of the regions I, II and 13a. (4) Still further, Fig. 6 of current Application showing the primary crystal grain boundaries in the channel region I includes regions not denoted between the LDD or offset regions II and the source/drain region 13a, and therefore the outer sides of the LDD or offset regions II do not directly contact the source/drain region 13a. While Fig. 5 of current Application shows that the outer sides of the LDD or offset regions II contact the source/drain region 13a, Fig. 5 does not show any primary crystal grain boundaries in the channel region I. Claims 3-5 depend on claim 1, and therefore claims 3-5 also fail to comply with the written description requirement.

5. Claims 6, 7 and 9-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Regarding claims 6 and 7, Applicants originally disclosed “lightly doped drain (LDD) or offset regions” recited in claim 6 or “offset regions” recited in claim 7 and “source and drain regions” where a width of the LDD or offset regions is less than a distance between primary crystal boundaries in Fig.

6 of current Application, but did not originally disclose that "the outer sides of the offset regions" directly contact "the source drain regions" in view of Fig. 6 of current Application, where there are regions, which are not denoted, between the LDD or offset regions II and the source/drain region 13a. Claims 9-11 depend on claim 7, and therefore claims 9-11 also fail to comply with the written description requirement.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 6, 7 and 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Oka et al. (US 6,184,541) (alternate interpretation).

Regarding claim 6, Oka et al. disclose a thin film transistor (TFT) (Figs. 1(a), 1(b) and 3(g)) comprising a channel region (8) (col. 3, line 42), source and drain regions (composite regions of 5 and a portion of 4 having a width of *D-d*) (col. 3, lines 38-40) respectively formed at opposite sides (left and right sides) of the channel region, lightly doped drain (LDD) or offset regions (portions of regions 4 having a width *d*) (col. 3, lines 60-66, and col. 4, lines 63-66), each comprising inner and outer sides, formed at respective opposite sides (left and right sides) of the channel region (8) and between the source and drain regions, the inner sides of the offset regions directly contacting the channel region, and the outer sides of the offset regions (portions of regions 4 having a

width *d*) directly contacting the source and drain regions (composite regions of 5 and a portion of 4 having a width of *D-d*), and a plurality of primary crystal grain boundaries (2 along vertical directions in Figs. 1(a), 1(b) and 3(g)) (col. 3, lines 36-37), wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate (3) (col. 3, line 36) are positioned in the channel, source and drain regions (8 and composite regions of 5 and a portion of 4 having a width of *D-d*) but not positioned in the LDD or offset regions (portions of regions 4 having a width *d*), and wherein a width (*d*) of the LDD or offset regions is less than a distance between two adjoining primary crystal grain boundaries (one rightmost primary crystal grain boundary in channel region 8 and another leftmost primary crystal grain boundary in region 4 on the right shown in Fig. 1(a)) because the LDD or offset regions are formed between two adjoining primary crystal grain boundaries.

Regarding claim 7, Oka et al. disclose a flat panel display device (col. 2, lines 27-29) comprising a thin film transistor (TFT) (Figs. 1(a), 1(b) and 3(g)) comprising a channel region (8) (col. 3, line 42), offset regions or *off-center regions* (portions of regions 4 having a width *d*) (col. 3, lines 38-39), each comprising inner and outer sides, formed at opposite sides (left and right sides) of the channel region, the inner sides of the offset regions directly contacting the channel region (8), source and drain regions (composite regions of 5 and a portion of 4 having a width of *D-d*) (col. 3, lines 39-40) respectively formed at the outer sides of the offset regions (portions of regions 4 having a width *d*) and directly contacting the outer sides of the offset regions, and a plurality of primary crystal grain boundaries (2 along vertical directions in Figs. 1(a), 1(b) and 3(g))

(col. 3, lines 36-37), wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate (3) (col. 3, line 36) are not positioned in the offset regions (portions of regions 4 having a width *d*), and wherein a width of the offset regions (*d*) is smaller than a distance between the primary crystal grain boundaries (2) because the offset regions are formed between two primary crystal grain boundaries, for example, one rightmost primary crystal grain boundary in the channel region 8 and another leftmost primary crystal grain boundary in the region 4 on the right shown in Fig. 1(a).

Regarding claim 9, Oka et al. disclose the flat panel display device according to claim 7.

The limitation "the polysilicon substrate is formed by a sequential lateral solidification (SLS) method" is merely a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966.

Regarding claims 10 and 11, Oka et al. further disclose for the flat panel display device according to claim 7 that the thin film transistor is used in an LCD device (col. 2, lines 27-29) (claim 10), and the primary crystal grain boundaries (2 along vertical directions in Figs. 1(a), 1(b) and 3(g)) are substantially perpendicular to a current direction (left-to-right or right-to-left direction) between the source and drain regions

(composite regions of 5 and a portion of 4 having a width of *D-d*) of the thin film transistor (claim 11).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1 and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oka et al. (US 6,184,541) (alternate interpretation).

Regarding claim 1, Oka et al. disclose a thin film transistor (TFT) (Figs. 1(a), 1(b) and 3(g)) comprising a channel region (8) (col. 3, line 42) having a plurality of primary crystal grain boundaries (2) (col. 3, lines 36-37), source and drain regions (composite regions of 5 and a portion of 4 having a width of *D-d*) (col. 3, lines 38-40) formed at respective ends (left and right ends) of the channel region, and offset regions or *off-center regions* (portions of regions 4 having a width *d*), each comprising inner and outer sides, one of which is formed between the channel region (8) and the source region and the other of which is formed between the channel region and the drain region, the inner sides of the offset regions directly contacting the channel region (8), and the outer sides of the offset regions (portions of regions 4 having a width *d*) directly contacting the source and drain regions (composite regions of 5 and a portion of 4 having a width of *D-d*), wherein the thin film transistor is formed so that the primary crystal grain boundaries

(2 along vertical directions in Figs. 1(a), 1(b) and 3(g)) of a polysilicon substrate (3) (col. 3, line 36) are not positioned in the offset regions.

Oka et al. differ from the claimed invention by not showing that a width of each one of the offset regions is smaller than a distance between the primary crystal grain boundaries formed in the channel region.

Oka et al. further disclose that the grain size of the polysilicon substrate (16 in Fig. 3(b)) is as fine as 1.0 ± 0.5 μm and the polysilicon substrate itself has high homogeneity (col. 4, lines 40-41).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that a width of each one of the offset regions (*d*) may be smaller than a distance between the primary crystal grain boundaries formed in the channel region, because *d* is smaller than a lateral grain size of polysilicon grains in which an offset region is formed, and the width of each one of the offset regions (*d*) may be smaller than a distance between primary crystal grain boundaries (distance between nearest neighboring primary crystal grain boundaries, or distance between next nearest neighboring primary crystal grain boundaries) formed in the channel region when the grain size of the polysilicon substrate is substantially uniform.

Regarding claim 3, Oka et al. disclose the thin film transistor according to claim 1.

The limitation "the polysilicon substrate is formed by a sequential lateral solidification (SLS) method" is merely a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. The patentability of a

product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966.

Regarding claims 4 and 5, Oka et al. further disclose for the thin film transistor according to claim 1 that the thin film transistor is used in an LCD device (col. 2, lines 27-29) (claim 4), and the primary crystal grain boundaries (2 along vertical directions in Figs. 1(a), 1(b) and 3(g)) are substantially perpendicular to a current direction (left-to-right or right-to-left direction) between the source and drain regions (composite regions of 5 and a portion of 4 having a width of *D-d*) of the thin film transistor (claim 5).

Response to Arguments

10. Applicants' arguments with respect to claims 1, 6 and 7 have been considered but are moot in view of the new grounds of rejection.

(1) Amended claims 1, 6 and 7 do not comply with the written description requirement as stated above. (2) The cross sectional view of Fig. 1(b) of Oka et al. is substantially identical to Fig. 6 of current Application, which shows a region interposed between each of an LDD or offset region II and a source/drain region 13a. (3) Applicants' arguments against the prior art rejection are based on a labeling of "source and drain regions" without Applicants specifically defining what can constitute "source and drain regions" such as a doping concentration. (4) Applicants' arguments may also be based on importing claim limitations from the specification, which is improper as stipulated in MPEP 2111.01. (5) As pointed out before, especially in Advisory Action

mailed February 9, 2011, Applicants cannot argue that the Examiner cannot use Oka et al. reference to reject claims because Oka et al. *simply* did not use the same labels as Applicants, when Fig. 1(b) of Oka et al. is substantially identical to Fig. 6 of current Application with different labels of source and drain regions. (6) Merriam-Webster dictionary defines "source" as "an electrode in a field-effect transistor that supplies the charge carriers for current flow" and "drain" as "an electrode in a field-effect transistor toward which charge carriers move". Therefore, the limitations "source and drain regions" do not necessarily suggest uniformly and highly doped regions, and the composite regions of 5 and a portion of region 4 having a width of *D-d* in Fig. 1(b) of Oka e al. can be referred to as a source region being capable of supplying charge carriers for current flow and a drain region toward which charge carriers move.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571)270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. K./
Examiner, Art Unit 2815
March 13, 2011

/Jay C Kim/
Examiner, Art Unit 2815